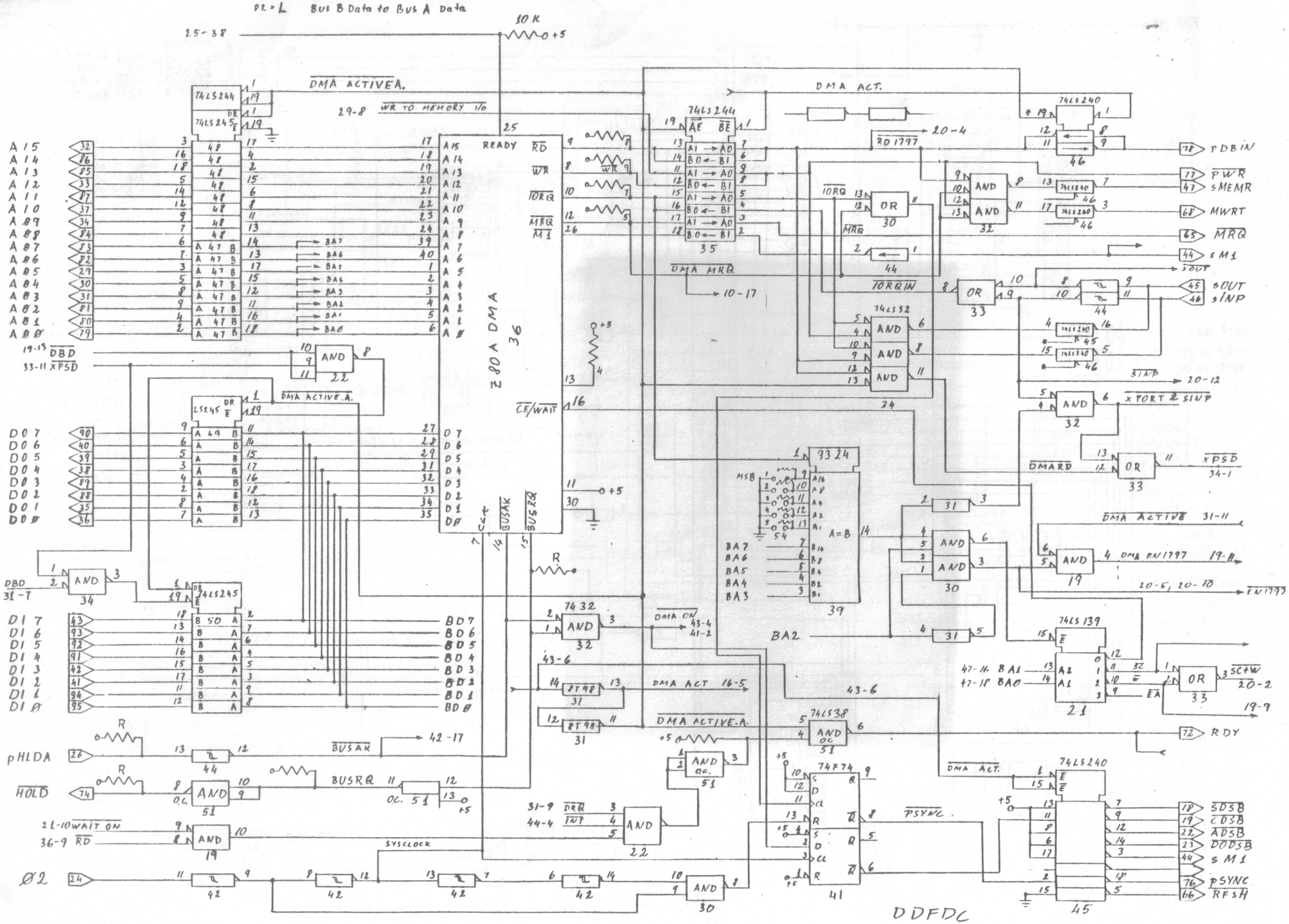
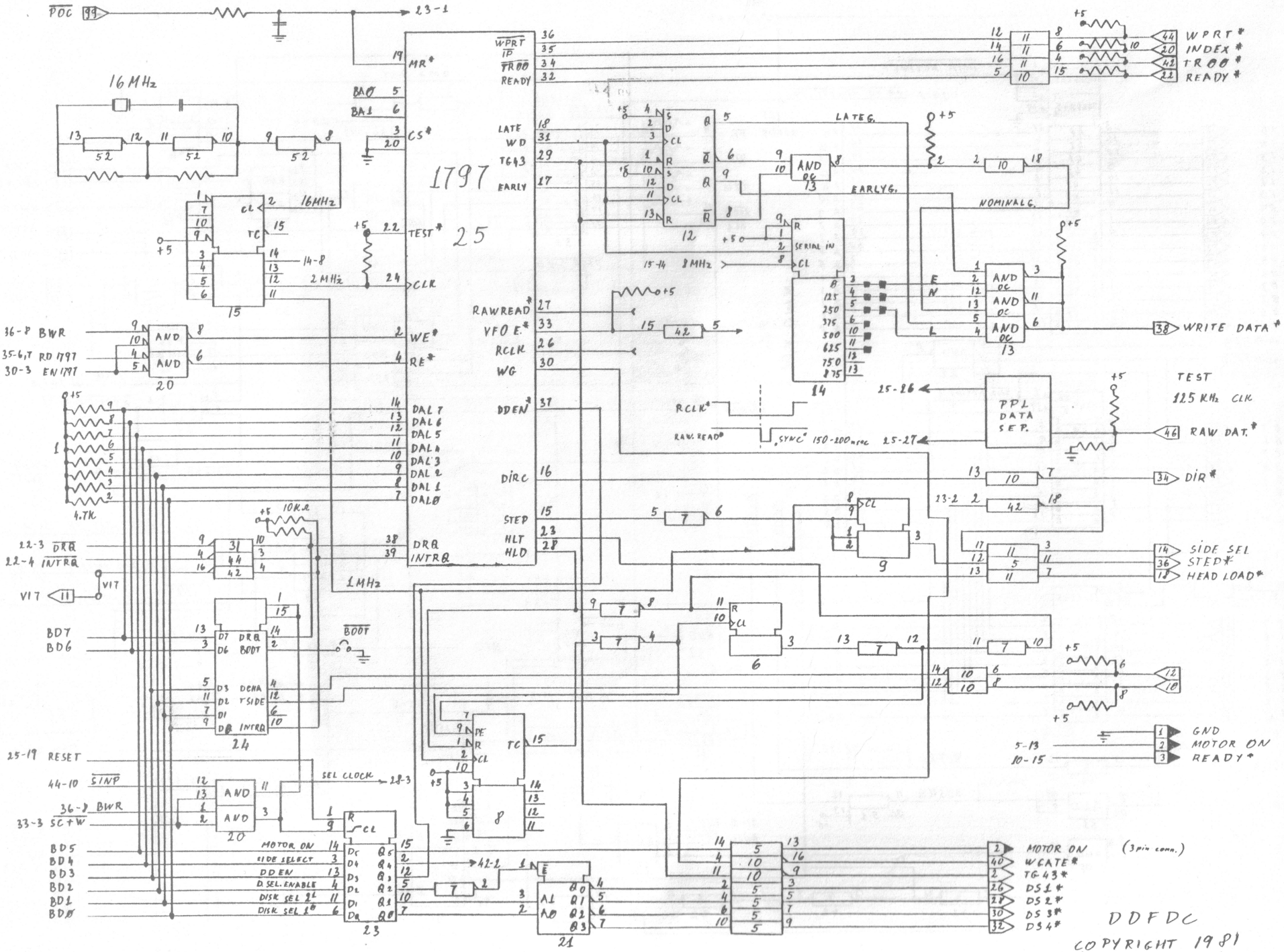
DR = H  Bus A Data to Bus B Data
DR = L  Bus B Data to Bus A Data




POC
23-1
16MHz
1797
25
MR*
BA0
BA1
CS*
TEST*
CLK
WE*
RE*
DAL 7
DAL 6
DAL 5
DAL 4
DAL 3
DAL 2
DAL 1
DAL0
DRQ
INTRQ
WPRT
IP
TR00
READY
LATE
WD
TG43
EARLY
RAWREAD*
VFO E*
RCLK
WG
DDEN*
DIRC
STEP
HLT
HLD
1MHz
2MHz
16MHz
36-8 BWR
35-6,7 RD 1797
30-3 EN 1797
22-3 DRQ
22-4 INTRQ
V17
BD7
BD6
25-19 RESET
44-10 SINP
36-9 BWR
33-3 SC+W
BD5
BD4
BD3
BD2
BD1
BD0
BOOT
SEL CLOCK
28-3
MOTOR ON
SIDE SELECT
DDEN
D SEL. ENABLE
DISK SEL 2*
DISK SEL 1*
42-1
LATEG.
EARLYG.
NOMINALG.
SERIAL IN
15-14 8MHz
14-8
PPL DATA SEP.
25-26
25-27
RCLK*
RAW READ*
SYNC 150-200 nsec
TEST
125 KHz CLK
RAW DAT.*
DIR*
23-2
SIDE SEL
STEP*
HEAD LOAD*
WRITE DATA*
WPRT*
INDEX*
TR00*
READY*
GND
MOTOR ON
READY*
5-13
10-15
MOTOR ON
WGATE*
TG43*
DS1*
DS2*
DS3*
DS4*
(3 pin conn.)
DDFDC
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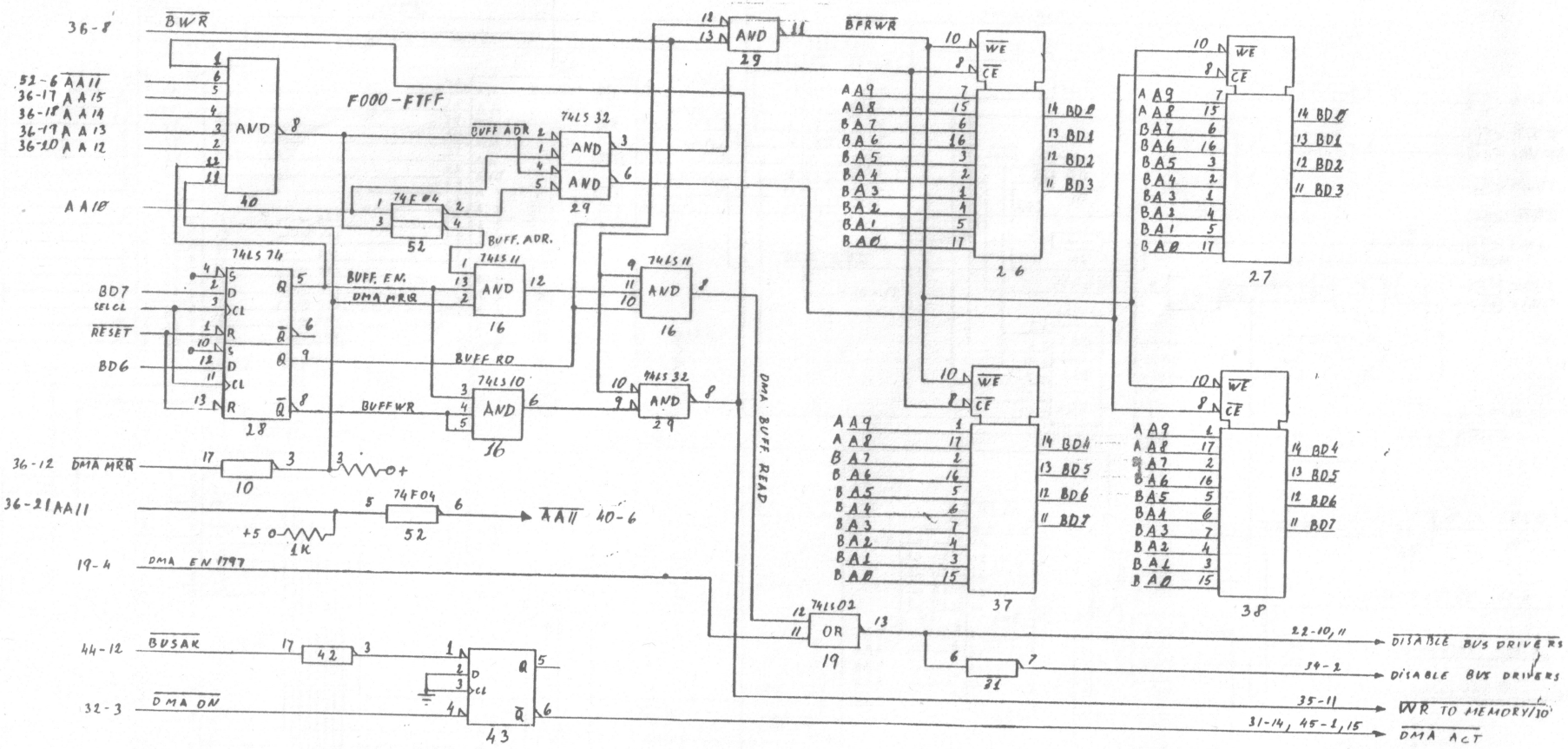
2 of 3




DD FDC

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